## REMARKS

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1-20 are pending in this application. Claims 16 and 20 stand rejected. Claims 1-12 are withdrawn from consideration as being directed to a non-elected invention. Claims 13-15 and 17-19 are allowed.

### Claim Rejection-35 U.S.C. §103

Claims 16 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over **Jamal et al.** (USP 6,724,813) in view of **AAPA** (Applicant's Admitted Prior Art). For the reasons set forth in detail below, this rejection is respectfully traversed.

The Examiner relies on Fig. 7 of the **Jamal et al.** reference, which illustrates a scrambling code generator that generates a "Gold" code using linear feedback shift registers[1].

More specifically, as shown in Fig. 7, the scrambling code generator includes two 41 bit linear feedback shift registers. The state of one of the shift registers is initialized with a set of parameters representing cellular system identification (SID), a cell identifier (CID), an access reference (AR), a signature (SIG), an access slot (AS), and a system frame number (SFN). The state of the other linear feedback shift register is initialized with all 1s. See col. 8, lines 61-63; col. 8, lines 66 - col. 9, line 4; and col. 9, lines 8-19.

[1] The general teaching of the use of linear feedback shift registers to generate a "Gold" code appears to be a known technique that was in use prior to the **Jamal et al.** reference.

As shown in Fig. 7, the scrambling code generator includes three exclusive or (XOR) gates. One of the XOR gates receives as inputs the outputs (i.e., LSB) of the linear feedback shift registers, and apparently outputs a scrambling code. The other two XOR gates are apparently used to provide respective feedback bits to the input (MSB) of the shift registers.

The Examiner's current position appears to be that **Jamal et al.** discloses all claimed elements except the "specific teaching that the logic circuit produces [a] matrix, and the matrix being used to form scrambling codes based on predetermined polynomial." See Office Action, pages 2 and 3, Item 3(a); and more particularly, page 3, lines 3-5. As best understood, the Examiner relies on the teachings of **AAPA** to show that the shift registers of **Jamal et al.** produce a matrix and generate a polynomial set for the scrambling code generator (see Office Action, page 3, lines 10-12.

More specifically, the Examiner reasons that "it is *well known* in the technology that a scrambling code generator comprises *feedback shift registers that generate matrix and polynomial set.*" [emphasis added] The Examiner apparently relies on the teachings of **AAPA** to support this position, asserting "AAPA teaches that the registers can be represented as a matrix after certain number of shift operations ([0036-0051]). And the registers generate a scrambling code sequence based on polynomial set ([0025-0027])." See Office Action, page 3, lines 6-10.

As set forth in the Manual of Patent Examining Procedure (MPEP) §2143.03 "To establish *prima facie* obviousness of a claimed invention, ***all the claim limitations*** must be taught or suggested by the prior art." *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). As will be discussed in detail below, it is respectfully submitted that the combination of **Jamal et**

**al.** and **AAPA** does not teach or suggest all claim limitations. Therefore, the rejection under §103 is improper and should be withdrawn.

First, the Office Action asserts that one of the linear feedback shift registers shown in Fig. 7 of **Jamal et al.** corresponds to the claimed "*storage circuit storing predetermined initial values.*" However, the claimed "storage circuit" is different from the linear feedback shift registers. The storage circuit of the claimed invention corresponds to the initial value buffer 22, which stores the initial value Ri shown in Fig. 13 of the present application, and is different from the shift register disclosed in **Jamal et al.** (see description in column 5, lines 56-67 of **Jamal et al.**).

Further, as discussed in detail below, it is submitted that **Jamal et al.** do not disclose or suggest the claimed "logic circuit" and the claimed "arithmetic circuit."

Arithmetic circuit

The Examiner apparently asserts that the exclusive OR (XOR) gate that receives the respective outputs of the linear feedback shift registers in **Jamal et al.** corresponds to the claimed "*arithmetic circuit that receives said matrix produced by the logic circuit as an input, multiplies said predetermined initial values stored in said storage circuit by said matrix produced by said logic circuit to compute a value of each code forming said sequence of scrambling codes, and outputs said sequence of scrambling codes*". See paragraph bridging pages 2 and 3 of the Office Action. In particular, the Examiner asserts "it is well known that XOR gate perform[s] multiplication operation." See Office Action, page 3, lines 1-2.

First, **Jamal et al.** does not disclose or suggest that the XOR gate that receives the outputs (LSB) of the linear feedback shift registers performs a multiplication operation. Second, contrary to the Examiner's assertion, it is not well-known that an XOR gate performs a multiplication operation. An XOR gate performs a logical operation on two binary inputs. The result of the logical operation is a logical 1 when one or the other, but not both, of the inputs is a logical 1. If both of the inputs are logical 0 or logical 1, the output will be a logical 0.

Third, it is well established that it is proper to rely on "well known" prior art , without supporting documentary evidence to support the Examiner's conclusion, *only* when the facts asserted to be well known are capable of instant and unquestionable demonstration as being well known. See MPEP §2144.03A. Moreover, it is well established that general conclusions concerning what is "basic knowledge" or "common knowledge" to one of ordinary skill in the art without specific factual findings and some concrete evidence in the record to support these findings will **not support an obviousness rejection**. See MPEP §2144.03B.

Finally, in accordance with MPEP §2144.03C, applicants traverse the Examiner's assertion that "it is well known that XOR gate perform[s] multiplication operation." It is submitted that an XOR gate does not perform a multiplication operation, and, as such, the assertion that it is "well-known" that an XOR gate performs a multiplication operation is incorrect. Therefore, in accordance with MPEP §2144.03C, the Examiner is requested to provide documentary evidence in the next Office Action to support the assertion that it is well-known that an XOR gate performs a multiplication operation.

In view of the above remarks, it is submitted that **Jamal et al.** does not disclose or suggest the claimed "arithmetic circuit". Moreover, as discussed in the previous response, **AAPA** does not disclose or suggest the claimed arithmetic circuit.

Accordingly, claims 16 and 20 patentably distinguish over the cited prior art for at least the reasons discussed above. However, claims 16 and 20 patentably distinguish over the cited prior art for the additional reasons discussed below.

Logic circuit

The Examiner asserts that a second of the linear feedback shift registers in **Jamal et al.** corresponds to the claimed "logic circuit" (see Office Action, page 2, fourth line from bottom). Please note, the Examiner does ***not*** contend that the second linear feedback shift register of **Jamal et al.** is a logic circuit "*producing a matrix by a predetermined operation, said matrix being used to determine a value of each code forming a sequence of scrambling codes based on a predetermined generating polynomial*". See Office Action, page 3, lines 3-5.

Instead, the Examiner reasons that because (1) "it is well known in the technology that a scrambling code generator comprises feedback shift registers that generate matrix and polynomial set", and (2) "the AAPA teaches that the registers can be represented as a matrix after [a] certain number of shift operations[s]", it would have been "obvious to one of ordinary skill in the art to recognize that the shift registers of Jamal et al. produce [a] matrix and generate [a] polynomial set for [a] scrambling code generator." See Office Action, page 3, lines 5-12.

First, it is submitted that there is absolutely no disclosure or suggestion in the **Jamal et al.** reference that either of the linear feedback shift registers produces a matrix. The Examiner

apparently recognizes this fact because the Examiner has not pointed out any portion of the **Jamal et al.** reference that discloses or suggests that either of the linear feedback shift registers produces a matrix. As noted in the paragraph directly above, one of the ways in which the Office Action attempts to support the position that either of the shift registers of **Jamal et al.** produces a matrix is by asserting that "it is well known in the technology that a scrambling code generator comprises feedback shift registers that generate [a] matrix and polynomial set."

However, because **Jamal et al.** does not disclose or suggest that the linear feedback shift register disclosed therein generates a matrix, and the Examiner has not provided evidence in the form of a reference to support the assertion that "it is well known ... that a scrambling code generator comprises feedback shift registers that generate [a] matrix...", applicants traverse this assertion. In accordance with MPEP §2144.03C, the Examiner is requested to provide documentary evidence in the next Office Action to support the assertion that it is well-known that linear feedback shift registers, such as those disclosed by **Jamal et al.**, generate a matrix.

The Examiner is reminded that it is well established that general conclusions concerning what is "basic knowledge" or "common knowledge" to one of ordinary skill in the art without specific factual findings and some concrete evidence in the record to support these findings will not support an obviousness rejection. See MPEP §2144.03B.

Second, as noted above, the other way in which the Examiner attempts to support the position that either of the shift registers of **Jamal et al.** produces a matrix is by asserting that "the AAPA teaches that the registers can be represented as a matrix after [a] certain number of shift operations[s]", it would have been "obvious to one of ordinary skill in the art to recognize that

the shift registers of Jamal et al. produce [a] matrix and generate [a] polynomial set for [a] scrambling code generator."

However, the portions of **AAPA** cited by the Examiner (i.e., [0036-0051]) teach that the respective values in registers 11-14 (Fig. 15) after being shifted a number of times can be ***represented by*** a matrix (see, e.g., sections [0042]-[0045]). Thus, **AAPA** teaches that the values ***stored*** in the shift registers after being shifted a number of times can be ***represented by*** a matrix. However, **AAPA** does not disclose or suggest that the shift registers 11-15 ***actually produce a matrix that is received by an arithmetic circuit.***

Accordingly, it is respectfully submitted that, contrary to the assertion in the Office Action, page 2, fourth line from bottom, the combination of references does not disclose or suggest that a second of the linear feedback shift registers in **Jamal et al.** corresponds to the claimed "logic circuit" producing a matrix. Therefore, it is submitted that the rejection under §103 is improper for these additional reasons and should be withdrawn.

## CONCLUSION

In view of the foregoing amendments and accompanying remarks, it is submitted that all pending claims are in condition for allowance. A prompt and favorable reconsideration of the rejection and an indication of allowability of all pending claims are earnestly solicited.

If the Examiner believes that there are issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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